

### 3-chip VFO / stabiliser / Frequency Counter

Written by Hans Summers

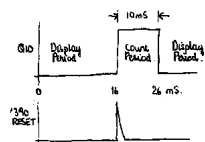
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Next I added a 74HC390 dual decade counter to the circuit. This effectively is half of my [2-chip Frequency Counter](#)

. The crucial thing, is that there is a lot of similarity between the timebase of the 2-chip frequency counter, and that of the 2-chip Huff & Puff stabiliser! With a little care, the frequency counter and the Huff Puff stabiliser can be made to share the SAME timebase! This allows me to build a combined device using just 3 IC's. It is important to use a 32.000KHz crystal, the usual 32.768KHz watch crystals are NOT Ok!

The counter has two digits of Binary Coded Decimal (BCD), i.e. 8 LED's. These are much easier to read than 8 bits of binary as on the [2-chip Frequency Counter](#), unless you are very good at mental arithmetic. For added functionality, I decided to try to build the counter to have two resolution modes. First, 00 - 99KHz with 1KHz resolution. This is the "course" mode. Next, a "fine" resolution mode measuring 0.0 - 9.9KHz with 0.1KHz resolution.



The 0.0 - 9.9KHz mode presented some timing complications. To measure frequency with 100Hz resolution requires a counting time of 10mS. Therefore I had to somehow generate this period, without adding further IC's. To do this, I added an AND gate fashioned out of 3 diodes and a resistor, to the outputs of the 74HC4060. Effectively, they count mS and cause the counter to be prematurely reset when it reaches a count of 26. During the last 10mS of this 26mS cycle, the Q10 output (pin 15) will be high. This can be used to gate the 74HC390 frequency counter! During the first 16mS, I arrange for the output LED's to be lit, and for them to be extinguished during the 10mS counting period. This is easy: just connect Q10 (pin 15) of the 74HC4060 to the commons of the LED's. I actually do this via a series of four 1N4148 diodes such that the voltage drop across the LED's is about right.

The 74HC390 also needs to be reset prior to each new count. I do this with a simple RC differentiator, which generates a very short spike when the counting period starts. The duration of this spike is only of the order of 10 or 20nS so doesn't affect the counting at all. I make the time constant as short as possible, whilst still allowing correct resetting of the 74HC390. This was a matter of trial and error.

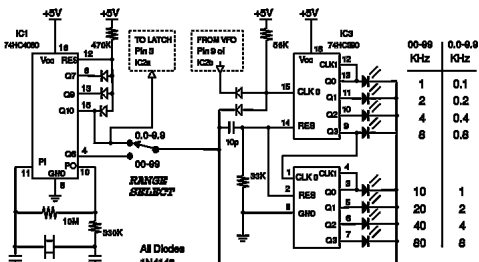
The new gating arrangement increases the frequency lock step slightly to 38.46Hz (1000 divided by 26).

The 00 - 99KHz mode is easy. All I do is connect the 74HC390 control signal (reset, gating, and display enable) to the 74HC4060's Q6 output (pin 4) which is oscillating at 500Hz, and naturally has the 1mS required high time already.

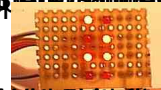
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For more information on this project, please visit the project page at [http://www.hanssummers.com/projects/vfo-stabiliser-freq-counter.html](#). The circuit is based on the 74HC290 decade counter and the 74HC280 parity generator. The circuit is powered by a +5V supply and includes various passive components and diodes. The frequency range table is provided on the right.



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